AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (original): A thin film transistor substrate comprising:

an insulating substrate;

a first thin film transistor formed above said insulating substrate, wherein said first thin film transistor comprises a first active layer formed above said insulating substrate, a first gate insulating film formed on said first active layer, and a first gate electrode formed on said first gate insulating film; and

a second thin film transistor formed above said insulating substrate, wherein said second thin film transistor comprises a second active layer formed above said insulating substrate, and a second gate insulating film formed on said second active layer, a second gate electrode formed on said second gate insulating film,

wherein a thickness of said second gate insulating film is larger than a thickness of said first gate insulating film,

wherein said second active layer has at least two impurity doping regions which overlap said second gate electrode,

wherein said first active layer has at least two impurity doping regions formed in a self-aligning manner with respect to said first gate electrode, and

wherein said second gate electrode comprises a semiconductor layer.

2. (original): The thin film transistor substrate according to claim 1,

wherein said second gate insulating film comprises said first insulating film and a gate cover film formed above said first gate insulating film.

3. (original): The thin film transistor substrate according to claim 1,

wherein said impurity doping regions formed in a self-aligning manner are formed so as to overlap said first gate electrode by 0.1 μm or less.

4. (original): The thin film transistor substrate according to claim 1,

wherein at least one of said impurity doping regions formed in a self-aligning manner with respect to said first gate electrode includes an LDD structure.

5. (original): The thin film transistor substrate according to claim 1,

wherein said impurity doping regions which overlap said second gate electrode are formed so as to overlap said second gate electrode by 2.0 μm or less.

6. (original): The thin film transistor substrate according to claim 1,

wherein at least one of said impurity doping regions which overlap said second gate electrode includes an LDD structure.

wherein said first gate electrode comprises a two-layer structure including a semiconductor layer and metal or metal silicide layer.

7. (original): The thin film transistor substrate according to claim 1,

wherein said first gate electrode comprises a two-layer structure including a semiconductor layer and metal or metal silicide layer.

8. (original): The thin film transistor substrate according to claim 1,

wherein said second gate electrode comprises a two-layer structure including a semiconductor layer and a metal or a metal silicide layer.

9. (original): The thin film transistor substrate according to claim 1,

wherein said second thin film transistor further comprises a third gate electrode formed between second active layer and said second gate electrode.

10. (original): The thin film transistor substrate according to claim 2,

wherein said second thin film transistor further comprises a third gate electrode formed on said first gate insulating film.

11. (original): A thin film transistor substrate comprising:

an insulating substrate;

a first thin film transistor formed above said insulating substrate, wherein said first thin film transistor comprises a first active layer formed above said insulating substrate, a first gate

insulating film formed on said first active layer, and a first gate electrode formed on said first gate insulating film; and

a second thin film transistor formed above said insulating substrate, wherein said second thin film transistor comprises a second active layer formed above said insulating substrate, and a second gate insulating film formed on said second active layer, a second gate electrode formed on said second gate insulating film,

wherein a thickness of said second gate insulating film is larger than a thickness of said first gate insulating film,

wherein said second active layer has at least two impurity doping regions which overlap said second gate electrode,

wherein said first active layer has at least two impurity doping regions formed in a self aligning manner with respect to said first gate electrode, and

wherein said second thin film transistor further comprises a third gate electrode formed between second active layer and said second gate electrode.

12. (original): The thin film transistor substrate according to claim 11,

wherein said third gate electrode is formed of the same material as said first gate electrode, and

wherein said third gate electrode has the same thickness as said first gate electrode.

13. (original): The thin film transistor substrate according to claim 11,

wherein said impurity doping regions formed in a self-aligning manner are formed so as to overlap said first gate electrode by 0.1 μm or less.

14. (original): The thin film transistor substrate according to claim 11,

wherein at least one of said impurity doping regions formed in a self-aligning manner with respect to said first gate electrode includes an LDD structure.

15. (original): The thin film transistor substrate according to claim 11,

wherein said impurity doping regions which overlap said second gate electrode is formed so as to overlap said second gate electrode by 2.0 μm or less.

16. (original): The thin film transistor substrate according to claim 11,

wherein at least one of impurity doping regions which overlap said second gate electrode includes an LDD structure.

17. (original): The thin film transistor substrate according to claim 11,

wherein said third gate electrode comprises a two-layer structure including a semiconductor layer and a metal or a metal silicide layer..

Claims 18-28 (canceled).